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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/370,508	08/06/99	SHARMA	U 20944.9000

EXAMINER	
ART UNIT	PAPER NUMBER
1765	4

020322
SNELL & WILMER
ONE ARIZONA CENTER
400 EAST VAN BUREN
PHOENIX AZ 85004-0001

IM52/0705

DATE MAILED: 07/05/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/370,508	SHARMA ET AL.	
	Examiner	Art Unit	
	DuyVu n Deo	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 14-17* is/are pending in the application.

4a) Of the above claim(s) *11-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claims *11-13* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-10, 14-17 in Paper No. 3 is acknowledged. The traversal is on the ground(s) that that examiner has cited no reasonable examples of a product, made by the claimed process, which is a non-semiconductor device. This is not found persuasive because allegations of different processes or products need not be documented as shown in MPEP under section 806.05(f). However, an example of other non-semiconductor product such as etching of a metal bulk or glass.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

2. Claim 2 recites the limitation "...prior to the step of removing the remaining anti-reflective coating" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 10, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 5,620,913) and Fu et al. (US 6,245,682).

Lee teaches a method for making a flash memory comprising: forming a silicon nitride overlying the substrate; depositing a layer of polysilicon overlying the silicon nitride layer;

forming a photoresist mask coating over the polysilicon; patterning the poly and the silicon nitride layer; removing the mask (col. 6, line 1-35). Unlike claimed invention, Lee doesn't describe forming an ARC over the poly layer. Fu teaches a method of poly etch wherein he teaches forming an oxide layer over the poly and a second silicon oxynitride over the oxide layer. They are patterned by using a resist layer. The silicon oxynitride layer is later removed with hot phosphoric acid (ab.; col. 4, line 30-35; col. 5, line 1-30). It would have been obvious at the time of the invention for one skill in the art to modify Lee in light of Fu because Fu teaches that the oxynitride as an ARC would helps to avoid the problem of distorted photoresist images due to reflections from the underlying semiconductor substrate; during the photolithographic definition of sub-micron poly gates (col. 2, line 60-68) and the oxide layer would help to protect the poly gate when the oxynitride is being removed by phosphoric acid (col. 5, line 10-20). Even though Fu doesn't describe removing the oxynitride before subjecting the layer of oxynitride to any temperature greater than about 400 degrees Celsius; the combined method above has the same steps as that of claimed invention; therefore, it would inherently not having any step that would subject the silicon oxynitride to any temperature greater than about 400 degree Celsius between the deposition and removing.

Fu also teaches of forming a layer of insulator on the edge of the poly prior to the step of removing the oxynitride (col. 5, line 11-19). The depositing of silicon oxide using TEOS source is well known to one skill in the art (please see Adkisson et al. col. 3, line 66-col. 4, line 1).

Referring to claim 3, since depositing and etching (by RIE) an insulating layer such as oxide layer is well known and available to one skill in the art, therefore, at the time of the invention, an oxide layer can be deposit on the pattern structure and the edge with an anticipation

of an expected result. As suggested by Fu, the insulator or oxide layer on top of the oxynitride would have to be removed in order to remove the oxynitride while the oxide layer protect the poly pattern.

5. Claims 7-9, 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Fu as applied to claims 1 and 14 above, and further in view of Cheung et al. (US 5,968,324).

Cheung teaches a method of forming oxynitride using SiH4 and N2O wherein the ratio between them is about 1.0 and Cheung further teaches that the refractive index, absorptive index, and thickness for different wavelengths can be controlled by varying the parameters and the rate at which the gases are introduced (col. 3, line 1-5; col. 4, line 1-33). It would have been obvious at the time of the invention for one skill in the art to deposit the oxynitride in light of Cheung because Cheung further teaches the parameters for the deposition of the oxynitride that is used by above prior art.

6. Claims 10, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al. (US 6,030,541).

Adkison teaches a method of forming a semiconductor device comprising: depositing an oxide layer from TEOS of about 100-1000 angstrom; depositing an oxynitride layer of about 100-2000 angstrom over the oxide layer; depositing a resist pattern over the oxynitride; patterning the oxide and the oxynitride layer; removing the oxynitride by using phosphoric acid (col. 3, line 50-col. col. 5, line 50). Unlike claimed invention, Adkison doesn't describe removing the oxynitride before the oxynitride is subjected to any temperature greater than about

400 degrees Celsius. Since Adkisson teaches the same steps as that of claimed invention, the method would inherently not having any step that would subject the silicon oxynitride to any temperature greater than about 400 degree Celsius between the deposition and removing the oxynitride layer.

7. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson as applied to claim 14 above, and further in view of Cheung et al. (US 5,968,324).

Cheung teaches a method of forming oxynitride using SiH4 and N2O wherein the ratio between them is about 1.0 and Cheung further teaches that the refractive index, absorptive index, and thickness for different wavelengths can be controlled by varying the parameters and the rate at which the gases are introduced (col. 3, line 1-5; col. 4, line 1-33). It would have been obvious at the time of the invention for one skill in the art to deposit the oxynitride in light of Cheung because Cheung further teaches controlling the parameters for the deposition of the oxynitride that is used by above Adkison in order to control the refractive index, the absorptive index, and the thickness of the oxynitride.

8. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al. (US 6,030,541) and Lee (US 5,620,913).

Unlike claimed invention, above method of Adkison doesn't describe forming a silicon nitride under the poly. Lee teaches a method of forming flash memory wherein a silicon nitride is formed under the poly (col. 6, line 1-5). It would have been obvious at the time of the invention to form a silicon nitride under the poly depending on the type of semiconductor device

being manufactured such as a flash memory taught by Lee. Adkisson's method of defining a pattern would be able to define a pattern having a silicon nitride under the poly with an anticipation of an expected result.

9. Wolf is cited to show that RIE of insulator (such as silicon oxide) is known and available to one skill in the art (pages 539-542).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n Deo whose telephone number is 703-305-0515.

DVD
June 29, 2001

ROBERT KUNEMUND
PRIMARY EXAMINER